SATES 25
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Mitigation of Interface Trap-Induced Bump Effects in p-Type MOS Capacitor

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Objective – The behavior of a SiOx/p-type Si MOS capacitor is explored under cryogenic conditions highlighting the impact of interface traps on its C-V characteristics. The work provides a framework for improving MOS capacitor functionality in low-temperature power applications.

Findings – At cryogenic temperatures, a bump effect emerges in the depletion region, linked to slow electron capture/emission dynamics of traps. The study reveals a memory effect tied to prior thermal and voltage history, alongside hysteresis and capacitance dispersion in the accumulation region.

Originality – **By applying voltage during the cooling process, the flat-band voltage can be manipulated, providing a strategy to reduce the bump effect and improve performance.**

Keywords – p-Type MOS capacitor, Cryogenic Temperatures, Interface Traps, Hysteresis Effect, Bump Effect, Flat-Band Voltage, Memory effect

1. Introduction

Cryogenic cooling, employed in systems like spacecraft and superconducting machines, offers a unique opportunity to integrate power electronics, typically operated at room temperature, directly into the cooled environment. By doing so, the need for thermal insulation to sustain room temperature operation is eliminated, resulting in a reduction in system complexity, size, weight, and costs. Cryogenic cooling also offers the advantage of performance enhancing of well know devices used for power application [1] like silicon based MOS by increasing critical parameters as breakdown voltage, mobility and consequently response time. Exploring the relationship between the material physics properties of power electronics MOS devices, influenced by fabrication processes, and their electrical behavior is crucial for fully optimizing system efficiency.

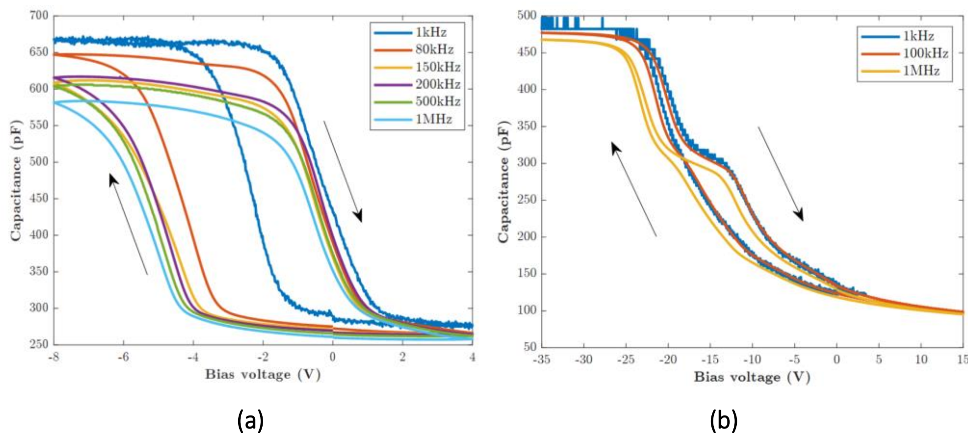
The fabrication process of MIS/MOS components can introduce trap energy levels within the insulator bandgap, leading to device instabilities such as leakage currents, increased switching losses, hysteresis, and slower response times, all of which negatively impact overall efficiency. To address these issues, samples fabrication, characterization and electrical and thermal studies were conducted to explore memory effects observed at cryogenic temperatures in Si/SiOx samples due to interface traps, with the goal of advancing techniques to mitigate these effects.

2. Capacitance vs Voltage behavior at room temperature and cryogenic temperature

Figure 1a shows the C-V curves at room temperature of a p-type MOS capacitor fabricated, where characteristic interface trap behavior, such as hysteresis and frequency dispersion in the accumulation capacitance, are observed [2]. Upon cooling, improvement is detected as the curves becomes less dependent of frequency, illustrated in Figure 1b. Nevertheless, new sources of instability arise, including a negative threshold voltage shift and a bump effect in the depletion region during the negative voltage sweep. A memory effect was also detected, where the first C-V measurement after cooling exhibited a bump three times larger than those in subsequent measurements, as shown in Figure 1b.

Assuming that this memory effect behavior is associated with certain trap energy levels with large capture time constant, which become accessible at higher temperatures but are typically unavailable at lower temperatures [3]. If this

memory effect can be somewhat controlled, this observation opens the possibility to mitigate the interface trap effects at cryogenic temperatures by regulating the voltage applied to the sample before or during the cooling process.



(a) (b)

Figure 1 : Measured capacitance behavior between 1kHz and 1MHz. a) T=293K. b) T=100K.

2.1 Influence of the applied voltage during cooling process

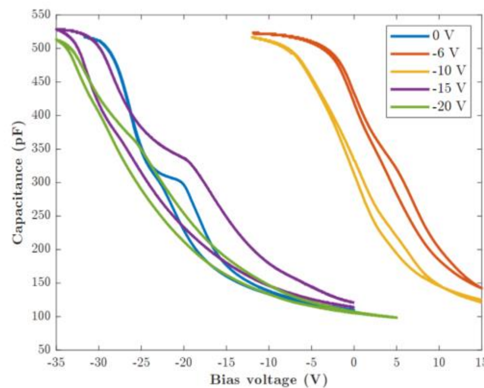


Figure 2 : T=100K. Measured capacitance behavior of the sample after post-processing with continuous voltage applied during the cooling process.

Fig. 2 shows the C-V curves at 100K for different voltages values applied during the sample's cooling, from -20V until 0V. When compared to the case where the sample cool down with 0V applied to it, it becomes possible to displace the flat-band voltage positively or negatively depending of the voltage applied. Analyzing the C-V curves it seems that the voltage necessary to positively increase flat-band voltage is strongly related to the strong accumulation region at room temperature and the bump beginning voltage at 100K. Reduction of the hysteresis and bump can be achieved as demonstrated by the curve -10V.

3. Conclusion

The occurrence of a memory effect, related to prior temperature and voltage conditions, is explored by applying a DC voltage to the samples during the cooling process. Post-processing C-V curves demonstrated the potential for reducing hysteresis, flat-band voltage shifts, and the bump effect at cryogenic temperatures.

Bibliography

[1] H. Gui *et al.*, "Review of Power Electronics Components at Cryogenic Temperatures," in *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 5144-5156, May 2020, doi: 10.1109/TPEL.2019.2944781.

[2] Aditya K. Bhat, Hyun-Seop Kim, Abhishek Mishra, Matthew D. Smith, Michael J. Uren, and Martin Kuball. Analysis of interface trap induced ledge in -ga2o3 based mos structures using uv-assisted capacitance–voltage measurements. Journal of Applied Physics, 135(19):195704, 05 2024.

[3] A. Goetzberger and J.C. Irvin. Low-temperature hysteresis effects in metal-oxide-silicon capacitors caused by surface-state trapping. IEEE Transactions on Electron Devices, 15(12):1009–1014, 1968